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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BELLO, AGUSTIN	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,704	BYERS ET AL.	
	Examiner	Art Unit	
	Agustin Bello	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1-3, 5-9, and 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corfield (U.S. Patent No. 4,682,323) in view of Hale (U.S. Patent No. 5,572,349).

Regarding claims 1 and 12, Corfield teaches generating at the signal generator a common clock signal (e.g. "master clock" of column 2 lines 60-66) and distributing the common clock signal over the free-space optical beam line to all processing units (column 2 lines 33-34); generating, at the signal generator based on said clock signal, a common synchronization signal and distributing the common synchronization signal over the free-space optical beam line to all processing units (e.g. "common output signal" of column 2 lines 3-11); maintaining in each processing unit, at least one timeslot counter (reference numeral 23 in the Figure; column 2 lines 12-22) synchronized to the clock signal (e.g. "master clock" of column 2 lines 60-66) and to the common synchronization signal (e.g. "common output signal" of column 2 lines 3-11 input to each circuit); generating at the signal generator corresponding timeslot map data (inherent in the "common output signal" of column 2 lines 3-11 input to each circuit and "master clock" of column 2 lines 60-66 since both allow the each input to be controlled so that it is only enabled during its respective time slot as described in column 2 lines 12-15), and distributing the message

pattern over the free space optical beam line to all processing units (column 2 lines 33-34), deriving an enable signal from the contents of the timeslot map to enable transmission of data into the beam line (inherent in the creation of a time division multiplexed signal wherein each input is enabled only for a respective time slot as described in column 1 lines 26-33 based on a received master clock signal or common signal either or which are used to derive timeslot map data) and deriving an enable signal from the contents of the timeslot maps to enable one or more receivers to extract data from the beam line (column 2 lines 12-22). Corfield differs from the claimed invention in that Corfield fails to specifically teach generating at the signal generator a message pattern containing a processing unit address and maintaining in each processing unit, a timeslot map based on the received timeslot map data associated with the address of the processing unit. However, as discussed above, the examiner believes that a time slot map is inherently transmitted via the common signal and master clock signal in that each circuit is capable of enabling transmission or reception during respective time slots based on the received common signal and master clock signal. In other words, the circuits of Corfield know which time slots to receive and in which time slots to transmit based on the received master clock signal and common signal, the master clock signal and common signal thereby providing a timeslot map of sorts which is maintained by the circuits of Corfield. Furthermore, Hale, in the same field of time division multiplexed optical communication, teaches addressing control messages to particular remote elements thereby controlling the timing of signals transmitted onto the network (column 4 lines 47-53) via the transmission of time slot map data (e.g. "timing" of column 4 lines 47-63). One skilled in the art would have been motivated to include address information for each processing unit in order to prevent control signals from being sent and received by an

unintended target (column 1 lines 27-37 of Hale). Furthermore, one skilled in the art would have been motivated to include time slot map data in order to provide overall synchronization for all elements of the system, a goal of both Corfield and Hale. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to generate at the signal generator a message pattern containing a processing unit address and maintain in each processing unit, a timeslot map based on the received timeslot map data associated with the address of the processing unit.

Regarding claims 2 and 13, the combination of Corfield and Hale teaches generating a timeslot sync signal (e.g. "master clock" or "common signal" of Corfield; "sync frame" of column 6 lines 28-30 of Hale), sending said timeslot sync signal to each of said processing units (inherent); receiving said timeslot sync signal at each of said sync pattern detectors (reference numeral 23 in the Figure of Corfield; reference numeral 52 in Figure 6 of Hale); and synchronizing said enable signal in each of said processing units (see column 2 of Corfield; see column 4 lines 54-62, column 7 lines 6-34 of Hale).

Regarding claims 3 and 14, the combination of Corfield and Hale teaches generating a frame sync pattern (e.g. "sync frame" of column 6 lines 28-30 of Hale), sending said frame sync pattern to each of said processing units (inherent); receiving said frame sync pattern at each of said frame sync pattern detectors (reference numeral 52 in Figure 6 of Hale), and synchronizing said timeslot counter in each of said processing units (see column 4 lines 54-62, column 7 lines 6-34 of Hale).

Regarding claims 5 and 15, the combination of Corfield and Hale teaches initializing and maintaining said timeslot maps using said geographic address input (e.g. phase-2 ranging section

R of Figure 2, the corresponding control signals from the OLT to the ONU, Hale's reference to "appropriately-addressed" portions of data in column 1 lines 33-36, and Hale's disclosure of "control channels addressed to specific ones of the ONUs" in column 4 lines 49-53).

Regarding claims 6, 7, 16 and 17, the combination of Corfield and Hale teaches the use of transmitting and receiving queues (column 3 lines 1-5 of Corfield). Furthermore, transmitting and receiving queues are well known in the art, and particularly well known in time division multiplexing systems.

Regarding claim 8, the combination of Corfield and Hale teaches enabling one or more receivers (reference numerals 20 in Corfield; reference numeral 24, 26 in Figure 3, reference numeral 108, 110 in Figure 8 of Hale) comprising enabling a plurality of receivers to simultaneous receive signals creating multicast channels (e.g. "point-to-multipoint" distribution of column 2 lines 7-10 of Hale).

Regarding claims 9 and 18, the combination of Corfield and Hale teaches that said signal generator includes guard band logic, said method further including the step of: periodically inserting guard bands into said beam line (e.g. "Quiet Phase" in Figure 2 of Hale).

Regarding claim 11, the combination of Corfield and Hale teaches distributing timeslots assigned to a given channel evenly throughout said timeslots to minimize latency (inherent in the time division multiplexing system of Hale and Corfield), said step of deriving an enable signal occurring serially across all of said processing units (e.g. "point-to-multipoint" distribution of column 2 lines 7-10 of Hale).

3. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corfield in view of Hale, as applied to the claims above, and further in view of Zikan (U.S. Patent No. 6,310,881).

Regarding claim 10, Hale differs from the claimed invention in that Hale fails to specifically teach updating said timeslot mapping to provide dynamic load balancing. However, updating time slot mapping in order to provide dynamic load balancing is well known in the art. Zikan in the same filed of time division multiplexing teaches as much (abstract and Figures 2 and 3). One skilled in the art would have been motivated to include updating of the time slot mappings in the system of Hale in order to provide dynamic load balancing in order to ensure the optimal use of the systems resources, namely bandwidth. Furthermore, Hale suggests updating time slot mappings in order to provide dynamic load balancing in that Hale teaches distribution of the bandwidth of the system flexibly by allowing timeslots to be mapped to any other timeslot (column 2 lines 7-18). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to allow updating of the time slot mappings in the system of Hale in order to provide dynamic load balancing.

Response to Arguments

4. Applicant's arguments with respect to claims 1-3 and 4-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Agustin Bello whose telephone number is (571) 272-3026. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AB

A. Bello

AGUSTIN BELLO
PATENT EXAMINER